THE FOLLOWING ARE THE ENGLISH TRANSLATION OF ANNEXES TO THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT (ARTICLE 34):

Amended Sheets (Pages 15-20)

CLAIMS

1. Field emission device, comprising:

- a cathode (22, 30),

- a porous insulating layer (26, 36), comprising open zones (40), which are pores of said layer,

- a conductive layer (28, 38, 48), called a gate layer, comprising at least one layer (45) of catalyst material for forming electron emitters and at least one layer (48) of a conductive material not catalysing the formation of electron emitters,

- electron emitters (29), in open zones (40) of the insulating layer and the gate layer.

2. Device according to claim 1, a resistive layer (24, 32) being arranged between the cathode and the insulating layer.

3. Device according to one of claims 1 or 2, the electron emitters being constituted by nanotubes (29) or nanofibres.

4. Device according to one of claims 1 to 3, the electron emitters being made of carbon.

5. Device according to one of claims 1 to 3, the electron emitters being made of a metallic material.

6. Device according to claim 5, the electron emitters being made of molybdenum or palladium.

7. Device according to one of claims 1 to 3, the electron emitters being made of an emitting semiconductor material.

8. Device according to claim 7, the electron emitters being made of silicon.

9. Device according to one of claims 1 to 8, the insulating layer being made of alumina.

10. Device according to one of claims 1 to 9, the open zones or the pores having a diameter between 5 nm and 25 nm.

11. Method for producing a field emission device, comprising:

- the formation of a cathode (22, 30),
- the formation of a porous insulating layer (26, 36), comprising open zones (40) that are pores in said layer,
- the formation of a conductive layer (28, 38, 48), called a gate layer, comprising at least one layer (45) of catalyst material for forming electron emitters and at least one layer (48) of a conductive material not catalysing the formation of electron emitters,

- the formation of electron emitters (29), in open zones of the insulating layer and the gate layer.

12. Method according to claim 11, further comprising the formation of a resistive layer (24, 32), between the cathode and the insulating layer.

13. Method according to claim 12, the resistive layer being made of amorphous silicon.

14. Method for producing a field emission device, comprising:

- the formation of a cathode (122, 222, 322),

- the formation of a first insulating porous layer (124, 224, 324), then a gate layer (128, 228, 328),

- the formation of a second insulating porous layer (126, 226, 326) and open zones (140, 240, 349) in said second insulating layer, the open zones being pores of said layer,

- the etching of the gate layer and the first insulating layer, through open zones of the first insulating layer (126, 226, 326),

- the formation of electron emitters, on catalyst zones, exposed at the base of the etched zones of the first insulating layer.

15. Method according to claim 14, comprising the formation of a catalyst layer (134) prior to the formation of the first insulating layer (124).

16. Method according to claim 15, comprising the removal of the second insulating layer (126), before or after the formation of electron emitters.

17. Method according to claim 14, comprising the deposition, at least in the etched zones (240, 340) of the first insulating layer, of a catalyst material (244, 344), after etching of the gate layer (228, 328) and the first insulating layer (224, 324).

18. Method according to claim 17, further comprising the removal of the second insulating layer (226), after deposition of the catalyst material.

19. Method according to claim 17, further comprising the removal of the second insulating layer (326), before deposition of the catalyst material (332), then the deposition of the latter in the etched zones of the first insulating layer (324) and on the non-etched zones of the gate (328).

20. Method according to claim 19, further comprising the formation of a metallic layer (330) on the catalyst layer (332) deposited on the gate.

21. Method according to one of claims 14 to 20, a resistive layer, for example of amorphous silicon, being arranged on the cathode (122, 222, 322).

22. Method according to one of claims 11 to 21, the emitters being nanotubes or nanofibres.

23. Method according to claim 22, the nanotubes being obtained by pure catalytic growth or with RF plasma.

24. Method according to one of claims 22 or 23, the emitters being made of carbon.

25. Method according to one of claims 11 to 24, the electron emitters being obtained by electrochemical deposition of an emitting metal.

26. Method according to one of claims 11 to 25, the insulating layer, or the second insulating layer, being produced from an aluminium layer.

27. Method according to claim 26, the open zones or the pores being produced by anodisation of the aluminium layer.

28. Method according to one of claims 11 to 27, the cathode being made of titanium nitride (TiN), molybdenum, chromium or tantalum nitride (TaN).

29. Method according to one of claims 11 to 28, the catalyst being made of nickel, or iron or cobalt or an oxide of these materials.